<table>
<thead>
<tr>
<th>PAD #</th>
<th>Name</th>
<th>Function</th>
<th>PAD #</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Gnd</td>
<td></td>
<td>73</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Comp_n</td>
<td>test comparator input -</td>
<td>74</td>
<td>Ctrl_rd_0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Vdd</td>
<td></td>
<td>75</td>
<td>Vdd</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Comp_p</td>
<td>test comparator input +</td>
<td>76</td>
<td>AD_0</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Gnd</td>
<td></td>
<td>77</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Comp_out</td>
<td>test comparator output</td>
<td>78</td>
<td>Trig_0</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Gnd</td>
<td></td>
<td>79</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Clear_test</td>
<td>test ring oscillator counter clear</td>
<td>80</td>
<td>Vdd</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Gnd</td>
<td></td>
<td>81</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>2G_test_out</td>
<td>test RO output (4096)</td>
<td>82</td>
<td>Clear_ADC</td>
<td>Clears ADC counter</td>
</tr>
<tr>
<td>11</td>
<td>Vdd</td>
<td></td>
<td>83</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Gnd</td>
<td></td>
<td>84</td>
<td>Ibias_comp</td>
<td>Comparator bias current</td>
</tr>
<tr>
<td>13</td>
<td>In_test</td>
<td>sampling cell test structure analog input</td>
<td>85</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Bias_left_test</td>
<td>sampling cell test input return</td>
<td>86</td>
<td>Vpol_cell</td>
<td>sampling cell's bias voltage</td>
</tr>
<tr>
<td>15</td>
<td>Gnd</td>
<td></td>
<td>87</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Trig_test</td>
<td>sampling cell test sample &amp; hold</td>
<td>88</td>
<td>Cext</td>
<td>External ramp input or internal ramp output</td>
</tr>
<tr>
<td>17</td>
<td>Gnd</td>
<td></td>
<td>89</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Vdd</td>
<td></td>
<td>90</td>
<td>Rp_return</td>
<td>ramp return</td>
</tr>
<tr>
<td>19</td>
<td>Gnd</td>
<td></td>
<td>91</td>
<td>Rp</td>
<td>Ramp active low, high clears ramp cap</td>
</tr>
<tr>
<td>20</td>
<td>Ctrl_rd_test</td>
<td>sampling cell test read</td>
<td>92</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>Gnd</td>
<td></td>
<td>93</td>
<td>Ibias_rp</td>
<td>ramp current</td>
</tr>
<tr>
<td>22</td>
<td>Write_test</td>
<td>sampling cell test write</td>
<td>94</td>
<td>Vdd</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>Vdd</td>
<td></td>
<td>95</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>Samp_out</td>
<td>sampling cell test output</td>
<td>96</td>
<td>VDL_out</td>
<td>output from VCDLs for delay lock</td>
</tr>
<tr>
<td>25</td>
<td>Token_out</td>
<td>output of token passing</td>
<td>97</td>
<td>Vdd</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>D=0&gt;</td>
<td>data out &lt;0:11&gt;</td>
<td>98</td>
<td>Vsw_p</td>
<td>sampling window control</td>
</tr>
<tr>
<td>27</td>
<td>D=1&gt;</td>
<td></td>
<td>99</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>D=2&gt;</td>
<td></td>
<td>100</td>
<td>Vsw_n</td>
<td>sampling window control</td>
</tr>
<tr>
<td>29</td>
<td>D=3&gt;</td>
<td></td>
<td></td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Gnd</td>
<td></td>
<td>101</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>D=4&gt;</td>
<td></td>
<td>102</td>
<td>VCP</td>
<td>VCDL control voltage</td>
</tr>
<tr>
<td>32</td>
<td>D=5&gt;</td>
<td></td>
<td>103</td>
<td>VCN</td>
<td>VCDL control voltage</td>
</tr>
<tr>
<td>33</td>
<td>D=6&gt;</td>
<td></td>
<td>104</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>D=7&gt;</td>
<td></td>
<td>105</td>
<td>Mck_return</td>
<td>write clock return</td>
</tr>
<tr>
<td>35</td>
<td>Vdd</td>
<td></td>
<td>106</td>
<td>Mck</td>
<td>write clock (40 MHz)</td>
</tr>
<tr>
<td>36</td>
<td>Gnd</td>
<td></td>
<td>107</td>
<td>Vdd</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>Gnd</td>
<td></td>
<td>108</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>D=8&gt;</td>
<td></td>
<td>109</td>
<td>Bias_left0</td>
<td>input return left &lt;0:3&gt;</td>
</tr>
<tr>
<td>39</td>
<td>D=9&gt;</td>
<td></td>
<td>110</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>D=10&gt;</td>
<td></td>
<td>111</td>
<td>Input0</td>
<td>analog input, channel 1</td>
</tr>
<tr>
<td>41</td>
<td>D=11&gt;</td>
<td></td>
<td>112</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>Gnd</td>
<td></td>
<td>113</td>
<td>Bias_right0</td>
<td>input return right &lt;0:3&gt;</td>
</tr>
<tr>
<td>43</td>
<td>Ck_cv</td>
<td>output of ring oscillator (4096)</td>
<td>114</td>
<td>Bias_left1</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>Gnd</td>
<td></td>
<td>115</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>VGLP</td>
<td>control ring oscillator (rising)</td>
<td>116</td>
<td>Input1</td>
<td>analog input, chan2</td>
</tr>
<tr>
<td>46</td>
<td>VGL2N</td>
<td>control ring oscillator (falling)</td>
<td>117</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>Vdd</td>
<td></td>
<td>118</td>
<td>Bias_right1</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>Gnd</td>
<td></td>
<td>119</td>
<td>Bias_left2</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td>Ctrl_rd_4</td>
<td>Read switch control &lt;0:4&gt;</td>
<td>120</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>Vdd</td>
<td></td>
<td>121</td>
<td>Input2</td>
<td>analog input chan3 w/ 50Ω</td>
</tr>
<tr>
<td>51</td>
<td>AD_4</td>
<td>Channel address, selects channel to be read &lt;0:4&gt;</td>
<td>122</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>Gnd</td>
<td></td>
<td>123</td>
<td>Bias_right2</td>
<td></td>
</tr>
<tr>
<td>53</td>
<td>Trig_4</td>
<td>Sample &amp; hold (high-sample, low-hold) &lt;0:4&gt;</td>
<td>124</td>
<td>Bias_left3</td>
<td></td>
</tr>
<tr>
<td>54</td>
<td>Gnd</td>
<td></td>
<td>125</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>Ctrl_rd_3</td>
<td></td>
<td>126</td>
<td>Input3</td>
<td>analog input chan4 w/ 50Ω</td>
</tr>
<tr>
<td>56</td>
<td>Vdd</td>
<td></td>
<td>127</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>AD_3</td>
<td></td>
<td>128</td>
<td>Bias_right3</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>Gnd</td>
<td></td>
<td>129</td>
<td>Vdd</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>Trig_3</td>
<td></td>
<td>130</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>Gnd</td>
<td></td>
<td>131</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>Ctrl_rd_2</td>
<td></td>
<td>132</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>Vdd</td>
<td></td>
<td>133</td>
<td>Vdd</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>AD_2</td>
<td></td>
<td>134</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>Gnd</td>
<td></td>
<td>135</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>65</td>
<td>Gnd</td>
<td></td>
<td>136</td>
<td>Ck_rd</td>
<td>read clock (40 MHz)</td>
</tr>
<tr>
<td>66</td>
<td>Gnd</td>
<td></td>
<td>137</td>
<td>Ck_rd_return</td>
<td>read clock return</td>
</tr>
<tr>
<td>67</td>
<td>Ctrl_rd_1</td>
<td></td>
<td>138</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>68</td>
<td>Vdd</td>
<td></td>
<td>139</td>
<td>Clear_token</td>
<td>clear token</td>
</tr>
<tr>
<td>69</td>
<td>AD_1</td>
<td></td>
<td>140</td>
<td>Tok_in</td>
<td>input of token passing</td>
</tr>
<tr>
<td>70</td>
<td>Gnd</td>
<td></td>
<td>141</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>71</td>
<td>Trig_1</td>
<td></td>
<td>142</td>
<td>Vdd</td>
<td></td>
</tr>
<tr>
<td>72</td>
<td>Gnd</td>
<td></td>
<td>143</td>
<td>Gnd</td>
<td></td>
</tr>
<tr>
<td>73</td>
<td>Gnd</td>
<td></td>
<td>144</td>
<td>Gnd</td>
<td></td>
</tr>
</tbody>
</table>
PAD/LAYOUT DIMENSIONS

- ALL UNITS MILLISECONDS
- BOXES REPRESENT BINDING AREAS ON PADS
- ALL DISTANCES MEASURED FROM CENTER OF BOXES

<table>
<thead>
<tr>
<th>PAD #</th>
<th>Dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-36</td>
<td>97 x 62</td>
</tr>
<tr>
<td>37-72</td>
<td>107 x 62</td>
</tr>
<tr>
<td>73-143</td>
<td>97 x 62</td>
</tr>
<tr>
<td>144</td>
<td>107 x 67</td>
</tr>
</tbody>
</table>

→ PAD ALL 100 MM CENTER TO CENTER
* EXCEPT PADS 143 & 144 → 102.5 MM

Top as in Layout