Write Clock (MCk) 40 Mhz

Trig_x – (asynchronous)

Write

Ctrl_rd_x

width ~ 2 us (time for ADC conversion)

Rp (ramp starts on hi-low switch)

ADC start

Read Clock (Ck_rd) 40 Mhz

AD_x

must trigger on a read clock leading edge, width= 2*delta t

Tok_in

width ~ 6.5 us (time to read out 256 cells)

Clear_ADC (high clears registers)

width ~ 8.5 us

Clear_token

width ~ 6.5 us

Repeat to read out other channels, if desired (AD_0-4)