Comparator, Part 2

Simulate response time of comparator with load.
- ramp: 0 to 1.2V in 2.4us
- IC: 60 uA
- Vref: swept from .2-1V in .1V steps

**Setup A:** comparator output loaded with 0.5 pF

**Setup B:** comparator output to AND (as it is for ADC conversion on chip. Other AND input from 2GHz ring oscillator, but kept at logic 1 for this simulation). Output of AND loaded with 1 pF
Results from A: comparator effectively stops working for $V_{\text{ref}} > 0.9\text{V}$

Results from B: AND acts like buffer – allows comparator to work for full range of ramp
Comparator Response – setup B

Results from B: Comparator time response from 2\textsuperscript{nd} plot on previous page showing non-linearity for large V\textsubscript{ref}. Error bars due to transistor variation shown in previous 'comparator' response & variation' post.