DC Tests: psTDC_01

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Wire-bonding
DC Board Goals

- Bonding of bare die to AC card is $$$$; need to make sure it’s a good investment.
  - DC board is simple and relatively cheap.

- Measure power, DC operating points

- Observe functionality:
  - Comparator
  - Sampling Cell
  - Ring Oscillator w/ 12 bit counter
  - Token Readout
  - Ramp Generator

- Compare results to simulation
DC Test Results

DC power

- Chip is drawing 250 mA @ 1.2 V – way too much
  - Measure 170 Ω from input pad to gnd/vdd. 120 pads in parallel gives roughly 5 Ω.
  - Why is there a connection at all?
  - Discovered that substrate is floating on packaged chips
    - possible short through substrate
DC Test Results

Sampling Cell
DC Test Results

Sampling Cell

Unexpected saturation for large $V_{in}$ ($V_{pol} = 0, 0.2 \text{ V}$)

The cell is fastest for high $V_{pol}$ but has more dynamic for a small $V_{pol}$
DC Test Results

Sampling Cell - leakage

1 - input LOW, write switch CLOSED
2 - input HI, switch CLOSED
3 - input HI, switch OPEN
4 - input LOW, switch OPEN

Simulations show leakage should decay to ground – not what we see.
This decay should be a lot faster
DC Test Results

Ring Oscillator

Operational to 1.5 GHz

Limited by 12 bit counter, which fails at this frequency
DC Test Results

Comparator

The good news:
- switches as expected

Not so clear:
- doesn’t reach +1.2 V
- only shows switching for **millisecond** time scale (output looks like capacitor for faster times, and is zero above that)
DC Test Results

Token Readout

Read clock of 400 KHz

**Token In** – pulse that straddles leading edge of clock

**Token Out** – output after token passed to 256 registers (one clock period per register).

Why is output so wide?
Summary

- Ramp doesn’t work yet, comparator is sketchy (could be working internally)
- Seeing signals ‘level off’ where we don’t expect
- Figure out substrate issue
- Maybe problems are related
- Bare dies sent to be bump bonded to Hawaii’s AC card