Design Review

*pS*TDC ver2*  
2-10-2010

included:
- ADC (minus comparator)
- Readout
- Timing Generation
- Trigger

Eric Oberla
ADC — ramp generator
ADC – ramp generator

with load of 2pF (conservative estimate), output of ramp buffer shows linearity ~75mV - 1V
ADC – d flip flop

- building block for Wilkinson ADC and readout registers
- this dff with CMOS switch = 1bit of 12 bit register
**ADC – 1 cell**

Overflow protection

Logic using 13th bit, CompOUT and Clear signals

When Reset dff→ 1, clock to registers is halted
ADC – 1 cell

Layout:

12 bit Register

12 microns

overflow protection

Read select logic
ADC – 1 cell

POST-LAYOUT simulation

clk freq = 2.85 GHz
ADC — 1 cell

POST-LAYOUT SIM - overflow protection

- clk input (freq = 2.85 GHz)
- comparator output (stays high)
- clk to register

counting stops when 13bit -> high
**ADC** — 64 cells

ring oscillator clock distribution
(more on that later)

12 bit data bus
ADC – 256 cells
(1 channel – 250x3200 micron^2)

ring oscillator clock distribution

tri-state output buffers:
CHAN_select_x = high
puts data on chip-wide bus
ADC – ring oscillator clock (ROck)

- one per channel
- the ROck freq. of each channel can be observed at output:
  ROck freq/4096 goes to common bus – output selected by CHAN_select_x
- ROck freq adjust via symmetrically controlled biases on NFET and PFET in delay cell

POST-LAYOUT simulation
ADC – ROck distribution

- attempted to simulate post-layout – too much for cpu

but, we can have confidence:

- buffer used to distribute ROck can drive ~100fF @ 2-3GHz from post-layout simulations
- layout was done such that each buffer drives < 50 fF
**Readout**—token unit

logic minimizes dead time w/o overlap:
Readout— token

new to version 2: `read_select` (2bit) – read cells 1-64, 65-128, 129-192 or 193-256

output bus settling time: again, too intensive for cpu, but parasitic extraction tells us the bus capacitance is 510 fF (This is before the tri-state buffer). Can simulate this from a schematic view:

--->

reading @ 40MHz should be no problem.

80MHz should also be possible
Readout– POST-LAYOUT simulation – read_select 1-64

other outputs (should be 0)

read clock (40MHz) and fan-out

token in

token out

a selection of the 1-64 outputs
Readout—

POST-LAYOUT simulation – read_select 129-192
Timing gen—delay unit

analog voltages
control sampling rate

--- to sampling window

--- to next cell
Timing gen—post layout of complete DL

POST-LAYOUT simulation

16-18 GHz
**Timing gen**— sampling window

- will have both fixed (2 channels) and variable (2 chan + 5th chan to observe)

fixed – 8 delay cells in length

variable window (indep. of sampling rate)
**Timing gen**—full DL with sampling window

POST-LAYOUT simulation (including long output traces) @ 13GS/s

variable window
(with VswN = VswP = 0.6V)

fixed window

M0(78.9ps, -3.269mV)
M2(928.5ps, -26.19mV)
M4(69.96ps, -7.479mV)
M6(610.1ps, 82.71mV)
**Trigger**— internal (with external option)

Variable delay (~7-20 ns nominal) between firing of trigger and hold signal to sampling cells

---

Variable delay (~7-20 ns nominal) between firing of trigger and hold signal to sampling cells

--- to output pad

--- to cells
Trigger—

- Trigger input & threshold signal to output pad
- Delayed signal to cells
- Input & threshold
- Signal to output pad

POST-LAYOUT simulation
POST-LAYOUT simulation – varying trigger threshold

with COMPbias = 50μA, DELAYbias = 0V (off)

- Trigger to cells
- Fails for two thresholds
- Input & thresholds
- Trigger signal to output pad