Design Review

'chastic*' chip  4-28-2010

included:
  - VCDL
  - RO w/ fast counter
  - ESD
  - I/O pads

Eric Oberla
*Chicago-Hawaii Application Specific Test IC (got any better ideas?)
Timing Generator Schematic for DLL and Sampling rate observation

Write strobe outputs -
(variable length)

Outputs of delay line to phase comparator

output of delay line to external
VCDL

upgraded delay unit -->
increased nominal sampling rate ~23 GS/s
New Ring Oscillator (using new delay units)

- compare frequency with that on 2\textsuperscript{nd} chip

- observe output/12 bits with counter made with fast dff's from 2\textsuperscript{nd} chip (~ 3GHz post layout)

- layout completed
I/O's

Digital Input – use this? or make new?
other pads (dig. out, analog in, etc) are also available

probably should decide on uniform pad dimensions

95 microns

63 microns (design min)
ESD protect.

Double diode on inputs -
require a discharge path in case of ESD
event on vdd or input => RC power clamp

dimensions:
120x100 um^2
ESD protect.

power clamp simulation

allows low resistance path from vdd to gnd if vdd spike > 2*vdd

spike on vdd

current through NFET switch

50 A! (maybe there should be a resistor in series with NFET switch?)