Most of these questions occur to me as I stare at the Full Tray Operational
Test - Block Diagram:
Reviewing Mircea Bogdan
November 16, 2010 presentation "PSEC Electronics Schedule"

Most of these questions occur to me as I stare at the Full Tray Operational

1) Is there a document describing the supported USB commands and data formats?

2) Does the System Clock 1to4 component exist on all digital boards so that any
board can be configured as a master to drive other digital boards?

3) Is there a length restriction on the LVDS cabling? How well matched need
they be to achieve a synchronous time standard?

4) Will the digital board have unique IDs which can be read via the USB.

5) If cables are used is there a length restriction on the cables between
the analog board and the digital board?

6) How is a test and/or calibration signal injected into the AB board?
   Could a special purpose board be made to mate with the front of the AB board?

7) Is there such a thing as daisy chaining the USB cable?
   Is there such a thing as a broadcast command on the USB cable?

8) How is gating based on an external trigger to be handled?

9) Can the front be connected easily to a set of 50 ohm cables to connect to
conventional PMT vi bnc or sma connectors?

10) Does the system work if I were to run the clock at 20 or 10 MHz rather than
40 MHz?

11) What are the estimated/predicted data and event rates sustainable for
the 4 USBs into a typical Linux PC?

12) Since there will be a temperature dependance to the calibration, how and
where do we digitize the temperature?

13) Are there parameters or configuration information to be downloaded to
the PSEC3 and FPGA chips?

Regarding the "full Tray Operational Test - Schedule"

14) In line 14 4 AB and 8 DB are manufactured, but in line 15 only 3 AB and 8 DB
are assembled!

15) An 8" module requires 2 AB and 4 DB for 80ch, what becomes of the other board
s?

16) The testing lines 17/18 appears to wait on line 15 to complete, but surely
as the 1st board pair is available testing should begin.

17) What is the line 17/18 test setup and testing actually consist of? What
additional hardward needs to be available to support.

18) I suspect testing and calibrating need to continue on a board pair while the
1st 1-tile tray is constructed and tested lines 21.22,23.
19) What are the 1-tile tray tests? pulser, radio active source, laser, cosmic rays, noise?

20) Does the Firmware, software Design include the software to go in the PC? What about software to archive data, an offline program to reprocess data and compare runs? How much of the software can be written and tested before real hardware is available?

21) Ultimately how many independant systems will be constructed and maintained? Who and where will they be used?

22) Will there be smaller (eg 4 channel) standalone systems for testing.

System count:
1) bench testing and repair at UofC
2) software development and testing
3) full tray 1 tile
4) partial tray for 1 tile

23) What about making more evaluation boards for testing and software development?