PSEC Electronics Status

The University of Chicago

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Figure 1. The first operational Tray incorporates 1 Tile. At each end, there is one Analog Board (AB), which has 10 ASICs and services 40 analog inputs. Each AB interfaces with two small Digital Boards (DB), placed right behind it, and attached with PMC connectors. Each DB communicates with 5 ASICs, generates a local trigger pulse, and reads all 5 data buses in parallel. After local processing and reduction, data are read out via USB. One DB generates the 40MHz clock for the whole Tray.
Changes

We made some changes in our plans to address the following:

- Reuse/Modify the existing PSEC3 Tester Card, to implement a Tray Operational Test with 1 ASIC (QFP), and without designing the Tray Digital Card yet?

- Reuse/Modify the existing PSEC3 Tester Card, to test PSEC3 flip chips, installed on small mezzanine cards?

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Figure 2. The existing PSEC3 Tester Card is modified to mate with the Tray Analog Card from Figure 1. This configuration can test up to 4 ASICs per Tray. The Tray Digital Card will be designed later.

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PSEC3 Flip Chip Test – Block Diagram

Figure 3. The new Tester Card will also be used to test PSEC3 Flip Chips placed on Mezzanine Cards.

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Conclusions

On the PSEC3 Tester Card we replace the PSEC3-QFP with a 152-pin Mictor connector, the same one used by the future Digital Card.

This new card will mate with the Tray Analog Card and service 1 ASIC.
- It will replace the Tray Digital Card (will test up to 4 ASICs per Tray).
- Requires no modifications to existing PSEC3 Tester firmware/software.

This new card will also accept mezzanine cards with 1 ASIC and 2 DACs.

Great savings in engineering time.

Plans:
- Modify PSEC3 Tester Card;
- Flip Chip Mezzanine Card design;
- Finish Analog Card specs (Input Circuit, OpAmps, etc.);
- Tray Analog Card design;
- Tray Functional Test.

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