CHAMP UC Testing

20 – April 2011
Updates

- Firmware completed for UC side of CHAMP
- Board up-and-running
- Still waiting on network analyzer for probe structures (tlines)
Voltage controlled ring oscillators

- 5-stage inverter + positive feedback
- 2 structures using regular/low_VT transistors
- Output fed to 12-bit counter divider made from fast, dynamic dffs

4.1 GHz attained with lowVT oscillator  ----> 

Counter/dff working at 4 GHz

![Graph showing frequency vs voltage with markers indicating different conditions]
Voltage controlled delay line

- 256-stage VCDL
- 2 structures using regular/low_VT transistors
Delay locked loop (debugging)