**Digital Card Requirements and Specs.**

**Requirements**
- Must provide power and control signals to the analog board for 5 PSEC chips
- Provide 5 clean write clock signals for PSEC chips (one clk each)
- Receive data from 5 PSEC chips and process the data (including vetoes and fitting)
- Final processed data will be sent to a central card for timing, fitting and final readout
- Waterproof?

**Clock distribution**

**Write Clock**
- A LVDS 40MHz clk is provided by the central card via CAT 5e/6 cable.
- Jitter cleaner (CDCE62005) can use the above clock or an onboard oscillator to make 10 single-ended CMOS signals (the JC has two inputs) Output RMS-Jitter < 1ps
  - Each PSEC ASIC receives one output clock of the JC
  - One output goes to FPGA on digital card
  - JC’s 3.3V output to be converted to 1.2V with SN74AVC1T45DBVR
    - From the Hawaii PS_TDC_01_eval Board

**Read clocks**
- Provided by an FPGA to the PSEC (40MHz)

**Other Clocks**
- Digital card FPGA has an onboard 120Mhz oscillator clock for internal logic.

**Power**
- Two power rails connect to the digital card from a power cable:
  +5.0VDC, +1.2VDC_PSEC
  +1.2VDC_PSEC is send directly to the analog card and is not used by the Digital card
  +5.0VDC is used by to create different rails on the digital card:
    +3.3VDC, +2.5VDC, +1.2VDC
  +3.3VDC is for the JC and is sent to the analog card for use in its DACs
  +2.5VDC is used for LVDS drivers in the FPGA
  +1.2VDC is for the FPGA’s output drivers for signals going to the PSEC ASICS
    Also used for FPGA core

**FPGA**
- The FPGA on the digital card will be a EP4CGX110DF27C7
  Manufacturer: Altera
  Family: Cyclone IV
  User I/O: 393 (BGA)
  Voltage Banks: 9
  Average Price: $320/ea
- Serial FLASH for storage of the FPGA programming file onboard
- Unused pins will be brought out to 2.54mm headers
USB
- USB2.0 will be connected to the FPGA for debugging and prototype readout without center card.

Communication
- Central card communication will be with LVDS via Cat5e/6 cables and RJ45 ports (see system requirements document)
- Analog card communication is via a SAMTEC QTH/QSH-120-01-L-D-A small pitch connector
  - 240 pins 0.5mm pitch
  - Center ground blade
  - Costs less than $20/ea
  - 8cm in length, surface mount

  - BNC connector for external trigger signal

Still needed
- Calculate total power consumed so regulators can be picked and traces can be sized
- Model the clock signals going to the analog board and try to keep SI intact.