Overview

Why a new board?

- Fix bugs = better PSEC4 stability
- Merge Rev. 1 Digital and Analog card to one board
- Use board-to-board connector instead of RF fingerstock compression connection = allows for readout of any system (i.e. Planacon MCPs)
- Add gain option for single p.e. mode
Mostly recycled design == limited firmware modifications

• Keep Central Card LVDS interface
• Fix D.C. USB for local board debugging
• 30 channels PSEC4 (5 chips)
• Same jitter cleaner (CDCE62005) and clock distribution
• Same FPGA
‘Analog Card’ == 5 PSEC4’s

Timing/calibration pulse injection to each PSEC4
PSEC4 block

Signals from input amps
High BW mux/switch used to switch Ch.6 of each PSEC4 to calibration pulse. Cal pulses injected via SMA (quick and easy). Try to generate these pulses on-board?
Input coupling
Input coupling

THS4303: fixed -10V/V gain amplifier
Operated from single 3.3V supply

AMP_ref = 1.5-1.8V from fixed regulator (from previous schematic)
THS4303 WIDEBAND FIXED-GAIN AMPLIFIER

FEATURES
- Fixed Closed-Loop Gain Amplifier
  - 10 V/V (20 dB)
- Wide Bandwidth: 1.8 GHz
- High Slew Rate: 5500 V/μs
- Low Total Input Referred Noise: 2.5 nV/√Hz
- Low Distortion
  - HD2: –65 dBc at 70 MHz
  - HD3: –76 dBc at 70 MHz
  - IMD3: –85 dBc at 100 MHz
  - OIP3: 34 dBm at 100 MHz
  - IMD3: –70 dBc at 300 MHz
  - OIP3: 27 dBm at 300 MHz
- High Output Drive: ±180 mA
- Power Supply Voltage: 3 V or 5 V

APPLICATIONS
- Wideband Signal Processing
- Wireless Transceivers
- IF Amplifier
- ADC Preamplifier
- DAC Output Buffers
- Test, Measurement, and Instrumentation
- Medical and Industrial Imaging

DESCRIPTION
The THS4303 device is a wideband, fixed-gain amplifier that offers high bandwidth, high slew rate, low noise, and low distortion. This combination of specifications enables analog designers to transcend current performance limitations and process analog signals at much higher speeds than previously possible with closed-loop, complementary amplifier designs. The devices are offered in a 16-pin leadless package and incorporate a power-down mode for quiescent power savings.

Specs @ +5V:

<table>
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<th>Specifications</th>
<th>1/4</th>
<th>1.1/3.9</th>
<th>1.2/3.8</th>
<th>V Max</th>
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<tr>
<td>Output voltage swing</td>
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<tr>
<td>Output current (sourcing)</td>
<td>180</td>
<td>170</td>
<td>165</td>
<td>160 mAh Min</td>
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<tr>
<td>Output current (sinking)</td>
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<tr>
<td>Output impedance</td>
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<th>Specifications</th>
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<tbody>
<tr>
<td>Specified operating voltage</td>
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<tr>
<td>Maximum quiescent current</td>
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<td>41</td>
<td>46</td>
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<tr>
<td>Minimum quiescent current</td>
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<td>27</td>
<td>25</td>
<td>23</td>
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<tr>
<td>Power supply rejection (PSRR +)</td>
<td>63</td>
<td>54</td>
<td>52</td>
<td>51</td>
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<tr>
<td>Power supply rejection (PSRR −)</td>
<td>65</td>
<td>58</td>
<td>56</td>
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</tbody>
</table>
Analog Card, pt. 2

Connector goes here...

SMAs for cal pulse injection

DACs = reused design
DACs = 2 ICs daisy chained
Added 3.3V for input amps
Layout progress

4.7”

7.3”
Layout: PSEC4, etc

MClk  DAC  PSEC4  10x Amps
Level shifters
Good idea to separate grounds in this fashion?

- No fast signals over ground isolation = no signal return problems
- Small patch makes DGND-AGND (DC) connection
- All other power planes separated
Schedule

• Make signal connector part & put in layout
• All other components are currently in place
• Hand route critical signals
• Try auto-router for remaining signals
• A final design review (?) w/ Gerber files, etc