Electronics – PSEC5 situation and plans
Status Report - 7/17/13

The University of Chicago
Electronics – PSEC5 situation and plans

Current work:

Getting familiar with the Cadence tool set and with the PSEC4 project; e.g. library management, PSEC4 schematics simulation, capture of simple schematics using the IBM design-kit.

Implement and simulate a VCDL schematic using the TSMC design-kit.
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VCDL schematic using the TSMC design-kit.

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Starting VCDL simulation.
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Questions/To Do List:

- Are we using the right kit, components, etc?
- Can we go all the way through with fully designing a simple ASIC now?
- Can we get a library of components?
- List of specs (ts, th, tp, etc.) for new logic components?
- Should start a PSEC5 Block Diagram showing new and reused blocks.
- What schematics from PSEC4 can be copied over and what schematics need to be redesigned?