Block Diagram – Writing of Sample & Hold Buffer

Clock = 40MHz, N = 100 => 2.5 us per Array @ 10Gsps

256 Primary Caps controlled by sw pointers at 100ps intervals
Each Primary Cap sends its analog value to N Buffering Caps
Buffers 1, 3,..., 2N-1 are written at successive sw pointers #130.
Buffers 2, 4,..., 2N are written at successive sw pointers #2.
Clock = 40MHz, N = 100 => 2.5 us per Array @ 10Gsps